REMARKS/ARGUMENTS

Claims 1-31 are pending in this application. Claims 1, 2 and 8 are being amended and claims 26-31 have been withdrawn from consideration. Applicants respectfully request re-examination, reconsideration and allowance of each of presently pending claims 1-25.

I. Rejection of Claims 1-5 and 8-25 Under 35 U.S.C. § 103

In paragraph 4 of the Office Action, claims 1-5 and 8-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (USPN 5,187,114), hereinafter "Chan '114", in view of Chan et al. (USPN 5,795,800), hereinafter "Chan '800". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Claims 1, 8 and 15 are the independent claims of the above-identified rejected claims.

*Claims 8-14 and 15-25

Independent claims 8 and 15 each recite the feature that both the PMOS transistor and the NMOS transistor are formed on an insulator substrate.

In particular, amended independent claim 8 recites the features of:

> An SRAM cell formed on an insulator substrate; and
>
> the cell comprising . . . at least a PMOS transistor and an NMOS transistor formed on said insulator substrate.

Similarly, independent claim 15 recites the features of:

> An SRAM cell formed on an insulator substrate; and
>
> the cell comprising: a first inverter having a first PMOS transistor and a first NMOS transistor.

On page 4, line 4 of the Office Action, the Examiner concedes that "Chan ('114), does not expressly disclose an insulating substrate." The Examiner then alleges that insulating substrates are well known in the art as demonstrated by Chan '800.

Applicants respectfully point out, however, that Chan '800 is CLEARLY limited to having only one of the NMOS or PMOS transistor formed over an insulating substrate. In column 2, lines 1-8, Chan '800 recites ". . . but this means the NMOS-to-PMOS spacing rules degrade density. For this reason the density of zero-power SRAM cells is only about half that of mainstream commodity SRAMs. One possible way to bypass the need for wells is to build *one of the device types* as an SOI (silicon-on-insulator) structure. This avoids the need for NMOS-to-PMOS design rules." Chan '800 continues, in column 2, lines 16-20, "The present application discloses a memory cell process in which a patterned buried oxide layer is formed under the PMOS devices by a high-dose high-energy oxygen implant. A hard mask screens this implant from the NMOS device areas." Chan '800 is therefore clearly directed to forming only one of the two devices (NMOS, PMOS) over an insulating area. This is done to avoid NMOS-to-PMOS spacing rules, the need to form wells, and Applicants respectfully submit that this absolutely *teaches away* from having both the NMOS device and the PMOS device over an insulating substrate as in the claimed invention.

Independent claims 8 and 15 are thereby clearly distinguished from the references of Chan '114 and Chan '800, taken alone or in combination.

Each of independent claims 8 and 15 also recite the feature of:

"a sidewall butted connection structure."

The sidewall butted connection structure feature is clearly and unambiguously defined in paragraph [0024] of the Specification. As defined in the Specification, the sidewall butted connection structure is a connection structure including a continuous silicide film that is formed by the encroachment and coupling of respective silicides formed by the silicidation between a metal film and silicon from two different, spaced

apart silicon sources. Neither of the references of Chan '114 or Chan '800 discloses or suggests this feature. Independent claims 8 and 15 are therefore further distinguished from the references of Chan '114 and Chan '800.

For reasons set forth above, the rejection of claims 8 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Chan '114 in view of Chan '800, should be withdrawn. Claims 9-14 depend from claim 8 and claims 16-25 depend from claim 15 and therefore the rejection of claims 9-14 and 16-25 under 35 U.S.C. § 103(a) should also be withdrawn.

*Claims 1-5

Independent claim 1 also recites the distinguishing feature that two semiconductor devices are formed over the insulator substrate. In particular, claim 1 recites the features of "*an insulator substrate,*" and "*a first semiconductor device formed on the insulator substrate,*" as well as "*a second semiconductor device formed on the insulator substrate.*"

As pointed out above with respect to independent claims 8 and 15, the combination of references of Chan '114 and Chan '800 do not disclose or suggest forming both semiconductor devices over an insulator substrate. Claim 1 is therefore distinguished from the references of Chan '114 and Chan '800, taken alone or in combination.

Amended independent claim 1 also recites the feature of the "sidewall butted connection structure," which is defined in the Specification, as above. As discussed with respect to independent claims 8 and 15, the sidewall butted connection structure is not disclosed or suggested by either Chan '114 or Chan '800. Amended independent claim 1 is thereby further distinguished from the references of Chan '114 and Chan '800, taken alone or in combination. The rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Chan '114 in view of Chan '800, should therefore be withdrawn.

Claims 2-5 depend from amended independent claim 1 and are therefore similarly distinguished from the references of record. Claim 2 has been amended to further point out distinguishing aspects of Applicants' invention. The rejection of claims 2-5 under 35 U.S.C. § 103(a), should be withdrawn.

II. Rejection of Claims 6 and 7 Under 35 U.S.C. § 103

In paragraph 5 of the Office Action, claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan '114/Chan '800 as applied to claim 1 and further in view of Chan (USPN 4,569,112), hereinafter "Chan '112". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Chan '112 has apparently been relied upon for providing thicknesses of the silicide layer referred to in claims 6 and 7, but does not make up for the above-stated deficiencies of the combination of Chan '114/Chan '800. Claims 6 and 7 depend from claim 1 which is distinguished from the references of Chan '114 and Chan '800, taken alone or in combination and therefore the rejection of claims 6 and 7 under 35 U.S.C. § 103(a), should also be withdrawn.

III. Amendment to the Specification

Paragraph [0024] of the specification has been amended to explicitly recite that which was inherent in the originally-filed specification and illustrated in the drawings.

CONCLUSION

Based on the foregoing, each of pending claims 1-25 is in allowable form and the application in condition for allowance, which action is respectfully and expeditiously requested.

The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

Dated: 01 November 05

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